In the Claims:

The claims are not being amended, but are re-presented below for the convenience of the Examiner.

1-26. (cancelled)

27. (previously presented) An integrated circuit comprising:

a gate array architecture;

said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions, said diffusion regions having partially overlying polysilicon landing sites, at least one forming both N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors, the relatively sized P-type diffusion regions being substantially adjacent;

successive rows of small diffusion regions followed by successive rows of larger-sized diffusion regions;

immediately successive rows within similarly-sized diffusion regions having opposite polarity; and

an interconnect connecting said smaller transistors as internal clock buffers.

28. (previously presented) The integrated circuit of claim 27, wherein a ratio between the two distinct transistor sizes is approximately one-third.

29. (previously presented) The integrated circuit of claim 28, wherein a ratio between capacitances of the larger and smaller relatively-sized transistors is approximately one-third.

30. (previously presented) The integrated circuit of claim 27, wherein said partially overlying polysilicon landing sites for the smaller and larger transistors are not connected.

31. (previously presented) The integrated circuit of claim 30, and further comprising an interconnect overlying said gate array architecture to connect the transistors of the gate array architecture to form a flip-flop having internal clock buffers.

32. (previously presented) The integrated circuit of claim 31, wherein the interconnect is further to connect the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.

33. (original) The integrated circuit of claim 32, wherein said gate array architecture is repeated in said integrated circuit.

34. (original) The integrated circuit of claim 32, wherein said integrated circuit is incorporated in a communications device.

35. (original) The integrated circuit of claim 32, wherein said integrated circuit is attached to a motherboard.

36. (original) The integrated circuit of claim 35, wherein said integrated circuit is incorporated in a personal computer.

37. (original) The integrated circuit of claim 36, wherein said personal computer comprises one of a laptop and a desktop computer.

38. (previously presented) An article comprising a storage medium having instructions stored thereon, said instructions, when executed, resulting in a capability to design a layout of an integrated circuit chip for fabrication, the integrated circuit chip including a gate array architecture, the gate array architecture comprising a plurality of N-type diffusion regions and P-type diffusion regions, said diffusion regions having partially overlying polysilicon landing sites, at least one forming both N-type and P-type transistors;

wherein the transistors are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors, the relatively sized P-type diffusion regions being substantially adjacent;

successive rows of small diffusion regions followed by successive rows of regular-sized diffusion regions;

immediately successive rows within similarly sized diffusion regions having opposite polarity; and

wherein said transistors are formed in said gate array architecture so that an interconnect disposed thereon connects said smaller transistors to form internal clock buffers.

39. (previously presented) The article of claim 38, wherein said instructions, when executed, result in a capability to design the layout of the gate array architecture, wherein a ratio between the two distinct transistor sizes is approximately one-third.

40. (previously presented) The article of claim 38, wherein said instructions, when executed, result in a capability to design the layout of the gate array architecture, wherein said partially overlying polysilicon landing sites for the smaller and larger transistors are not connected.

41. (previously presented) The article of claim 40, wherein said instructions, when executed, result in the capability to design the layout of an interconnect overlying said gate array architecture.

42. (previously presented) The article of claim 41, wherein said instructions, when executed, result in the capability to design the layout of an interconnect overlying said gate array architecture, wherein said interconnect couples the transistors of the gate array architecture to form a flip-flop having internal clock buffers.

43. (previously presented) The article of claim 42, wherein said instruction, when executed, result in the capability to design the layout of an interconnect overlying said gate array architecture that connects the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.

44. (previously presented) The integrated circuit of claim 32, wherein most of said smaller transistors are used for internal clock buffers.

45. (previously presented) The integrated circuit of claim 32, wherein substantially all of said smaller transistors are used for internal clock buffers.

46. (previously presented) The article of claim 43, wherein said instructions, when executed, result in the capability to design the layout of an interconnect overlying said gate array architecture so that most of said smaller transistors are used for internal clock buffers.

47. (previously presented) The article of claim 43, wherein said instructions, when executed, result in the capability to design the layout of an interconnect overlying said gate array architecture so that substantially all of said smaller transistors are used for internal clock buffers.